

when the lower 2-bit data of the pre-pit byte is the same as the reference pattern 00, the low bit is set to high level.

16. A pre-pit decoding circuit for receiving a pre-pit signal and a wobble signal and outputting a pulse signal and a new pre-pit signal, comprising:
 - 5 a pulse generating unit for generating the pulse signal, wherein the pulse signal rises substantially at the same time as the wobble signal rises;
 - an extension unit for generating an extension signal which rises substantially at the same time as the pre-pit signal rises and falls substantially at the same time as the pulse signal falls; and
 - 10 an AND-operation unit for generating the new pre-pit signal by doing an AND-operation on the extension signal and the pulse signal.

ABSTRACT OF THE DISCLOSURE

A pre-pit signal decoder includes a shift register, a pattern comparator, a counting unit, an in-sync signal generating unit and a protection unit. The register receives serial pre-pit bits and converts them into a parallel pre-pit byte. The comparator generates an odd sync bit, an even sync bit, a low bit, and a high bit according to the pre-pit byte and receives a disable signal to operate when the disable signal is not enabled. The counting unit generates a counting value, which marks oddness/evenness of frames of the pre-pit bits and sequence of wobble signals in the frames, according to the odd sync, even sync, low and high bits. The signal generating unit generates an in-sync signal according to the odd

sync, even sync, low, and high bits. The protection unit receives the counting value and the in-sync signal to thereby enable the disable signal at positions where the pre-pit bits impossibly exist according to the counting value. The decoder controls operations of the pattern comparator according to the disable signal of the

5 protection unit so as to reduce the error rate.